White paper on the future of atomic-level processing

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1 Executive summary

Atomic-level control of materials processing will be needed in the semiconductor industry within the next 5-10 years, and will be a powerful enabling technology for other high-tech manufacturing sectors. This will be possible if atomic-level precision can be achieved with the traditional fabrication steps – deposition, patterning and etching. There is therefore a strong need for research now into how the current concept of atomic layer deposition may be developed into selective-area patterning and atomically controlled etching.

2 Contents

3 Introduction to current state of the art

Atomic layer deposition (ALD) is a unique technique for growing ultra-thin films that is enabling new developments in high-tech manufacturing sectors such as electronics, energy and coatings. A wide range of materials can currently be deposited by ALD, including oxides, nitrides, sulfides, metals, organic and hybrid organic-inorganic materials. Unlike other chemical vapour deposition methods, ALD works by sequentially exposing a substrate to precursor gases one at a time, through rapid gas-pulsing or substrate displacement. This allows finer control of film thickness and the ability to uniformly coat all surfaces of a three-dimensional object, yielding a level of sub-nanometer precision with ALD that is unparalleled by other techniques.

ALD is now used in high-volume manufacturing. According to one of the world-leading companies in the field,[1]

> "ALD is now firmly established as a key enabling technology. Today, ALD has become a critical technology for the manufacture of virtually all leading-edge semiconductor devices. The leading customers in our industry have already ramped several device generations based on our ALD equipment – for high-k metal gate applications in logic and foundry and for multiple patterning applications in the memory sector."

4 Future market needs in atomic-level processing

The information economy is based on continual increases in the volume, speed and energy efficiency for data transfer, processing and storage. This in turn is based on continual down-scaling of semiconductor devices (*Moore's Law*) and new device concepts (*Beyond Moore*), both of which mean that manufacturing is becoming more challenging with every new device generation. There are three main approaches to achieving scaling and each comes with its own process challenges:

1. Scale down laterally into the nanometer regime (e.g. sub-10 nm patterning), meaning that process tolerances are in the atomic scale;
2. Exploit the third dimension (e.g. gate-all-around transistor or 3D-NAND memory), if materials can be processed in high aspect ratio features;
3. Integrate new materials with higher performance, if the new materials can be synthesized in a fab-compatible process.

The semiconductor industry is thus facing an urgent and long-term need for improved process technologies that have the following characteristics:

- ability to add or remove material at location of choice;
- atomic-scale control of material thickness and of process drift;
- ability to coat three-dimensional (3D) structures;
- compatible with existing manufacturing process;

- can be extended to novel materials.

ALD is unique in being able to meet some of these requirements, but to fulfil all the requirements will need further R&D (section 5).

One major reason for urgency is the delayed introduction of extreme ultra-violet (EUV) lithography in the semiconductor industry, which was originally planned for patterning at the 32 nm logic and memory nodes, but has now slipped to possible introduction at the sub-10 nm nodes. Through double-patterning, ALD can extend the use of current lithography. In addition, area-selective ALD can potentially replace some patterning steps entirely. 'ALD-enabled patterning' will thus likely co-exist with EUV lithography.

Atomically-precise process technologies can also be used for manufacturing in non-semiconductor sectors, enabling new functionality in a variety of mass-produced items. This is emphasized by the EuMaT technology platform: "Manipulation at the molecular level promises the development of advanced tailor-made (functionalized) materials with a combination of properties that outperform existing materials." For instance, sectors with particularly strong needs for atomic-level processing are:

- renewable energy (nanostructured fuel cells, solar cells, batteries, super-capacitors and photo-catalysts);
- medical applications (targeted and delayed drug delivery);
- photonics (multilayer structures for lasers, lighting, plasmonics and displays).

5 Future R&D directions in atomic-level processing

Atomic layer deposition (ALD) shows promise as a platform for future atomic-level process technologies, since it is proven to already meet some of the required characteristics (thickness control, pinhole-free and 3D coating, compatible with manufacturing line). To address all of the future market needs and transform ALD into a comprehensive platform for atomic-level processing, sustained R&D will be needed. Two key areas for future research have recently been identified and are now urgently needed by front-runner companies like Intel, IBM, Lam Research and Applied Materials: (1) atomic layer etching[2,3] and (2) selective area deposition.[4]

5.1 Atomic layer etching

Currently, plasma etching continues in a relatively uncontrolled way until interrupted by masks or etch stops. The idea of atomic layer etching (ALEt) is that *the process itself* should stop after the removal of one atomic layer of the target material. This would bring a totally new degree of control to material processing, as well as lowering cost by removing the need for etch stops.

Conceptually, an ALEt process can be thought of as a self-limiting ALD cycle operating *in reverse*, as shown in Figure 1, but there are many challenges to realizing this in practice (see below).

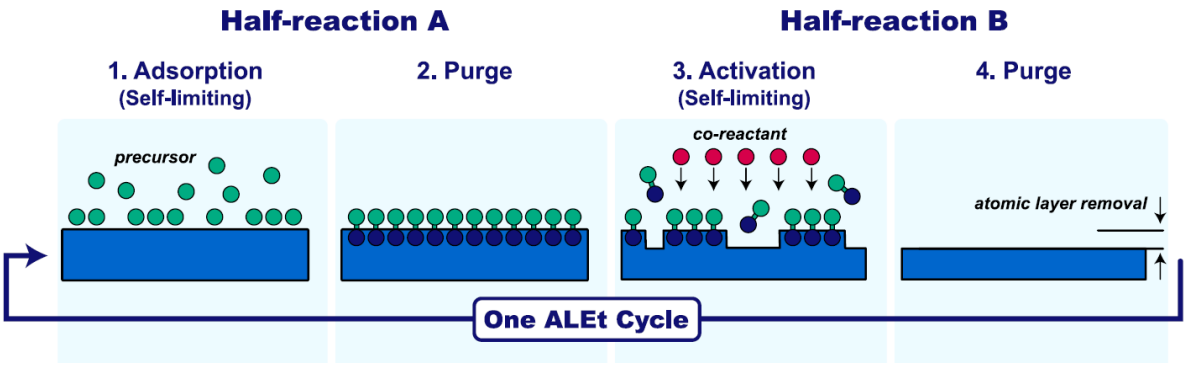

Figure 1: Schematic representation of the chemistry required for atomic layer etching; from Ref 5.

Future applications that depend on ALEt:

By analogy with ALD, a thermally-driven ALEt process could etch all parts of a nanostructure isotropically, even at high aspect ratios. Damage to the substrate (such as roughening) should be lower than with plasma. Controlled isotropic etching of this sort is needed to process nanowires for devices such as gate-all-around transistors and vertical NAND flash memories.

In other cases however, there are stringent temperature limits on some processes (*e.g.* <150°C for back-end metallization). Self-limiting plasma-based ALEt would therefore be useful for anisotropic etching at low processing temperatures. This is needed for certain nano-patterning applications (*e.g.* direct pattern transfer from resist).

Greater control of plasma conditions (*e.g.* separation of radical and ion fluxes) may allow surface reactions to be precisely controlled through the process time. Such 'quasi-ALEt' would enable the fabrication of self-aligned contacts.

It is proposed that cycles of ALD and ALEt can be combined so as to achieve 'atomic scale lithography' and thus deliver a multiple of the current lithographic resolution (*e.g.* double patterning).

New ALEt processes are also deemed necessary for beyond-CMOS technology nodes relying on 2D materials.

Research challenges for new ALEt process chemistry:

- Development of self-limiting etch processes for wider range of substrate materials;
- Design and synthesis of etchant chemicals for plasma and non-plasma-based ALEt that can be safely used in mass production;
- Modelling of etch chemistry and interaction of etchants and plasma with surfaces;

- Understanding the chemistry 'rules' that are required for AlEt.

Challenges in developing ALEt process equipment:

- Fine control of plasma conditions, including afterglow in pulsed plasmas;
- Development of specific plasma sources (single-source or microplasma arrays);
- Roll-to-roll ALEt equipment for flexible electronics;
- Sensitive control of ion energies in etching to reduce damage;
- Advanced gas-inlet designs for very uniform and ultra-fast precursor injection;
- Measurement and control of wafer surface temperature *in situ*.

5.2 Selective area deposition or etch

The goal of selective area processing is to achieve different processing of different substrate materials that are adjacent to one another, despite being exposed to the same processing conditions. This would mean that a substrate would need to be patterned only once, with subsequent selective area steps propagating that pattern with fidelity.

Area-selective ALD and ALEt for various material/substrate combinations would therefore enable nanostructures of arbitrary shape and composition to be built with atomic precision. However it is clear that developing a process for each pair of material/substrate combinations will need a tremendous experimental and modeling effort, especially in the area of novel precursor chemistries.

Currently, most approaches for selective-area ALD rely on the blocking of ALD growth using self-assembled monolayers (SAMs) or on local activation of the ALD growth (Figure 2). However, some materials can only be grown with the help of plasma, which damages SAM blocking layers. In addition, blocking layers and activation layers have limited lateral resolution, which will not be adequate for downscaling device dimensions below 10 nm. This motivates research into *inherently* selective ALD, exploiting differences in nucleation on different substrates. Another possible approach is to combine ALD and ALEt, so as to amplify their selectivity.

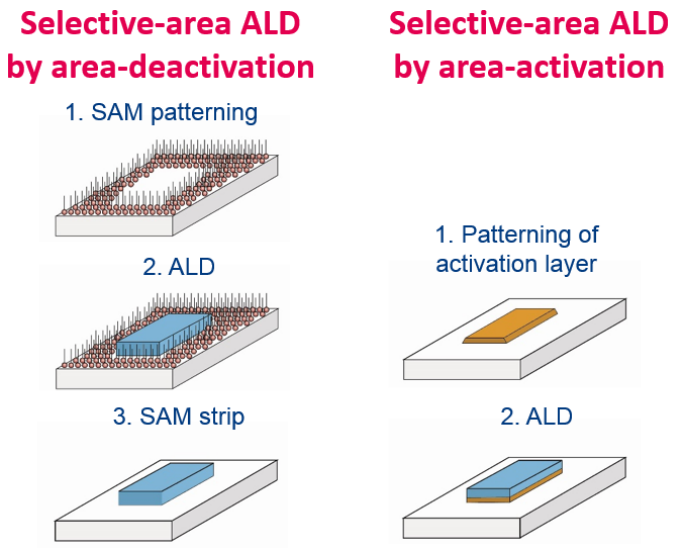

Figure 2: Schematic representation of process flows for two indirect approaches towards selective-area ALD; from Ref 6. By contrast, inherently area-selective ALD (not shown) would exploit the different nucleation chemistry at different substrate areas.

Applications that will be enabled by selective-area processing:

- Fewer lithographic steps and less severe mis-alignment errors in semiconductor fabrication (see next paragraph);
- Hermetic packaging for MEMS chips;
- Cross-point memory technologies (*e.g.* RRAM, PCRAM, STT-MRAM).

The need for selective processes (both deposition and etch) is increasing dramatically with the transition to smaller and smaller electronic devices (*e.g.* logic devices shrinking from 10nm to 7 nm to 5 nm) and 3D integration (3D NAND, FinFET to 3D gate-all-around transistor). Already today, one of the main challenges of conventional lithographic patterning is to align the different layers from multiple lithographic steps. Mis-alignment errors at edges and corners are projected to be a severe limit on future downscaling. An alternative would be to use selective area ALD or ALEt to deposit or etch material *only where needed* on the existing pattern, removing the need for additional lithographic steps.

Key challenges for research in selective-area processing:

- Understanding how different substrates affect ALD kinetics;
- In-situ process diagnostics and characterization of nanoscale thin films;
- Understanding which surface defects affect the selectivity of the ALD growth.
- Extend selective-area ALD to a wider range of materials.
- New reagents that work at the low deposition temperatures needed for selectivity;
- How to combine the high throughput of chemical vapour deposition (CVD) with high substrate selectivity;
- Current lack of understanding of interfaces, corners and edges, which are becoming dominant at the nanoscale.

5.3 Complementary areas for research

Materials deposited with ALD can give unique impetus to research in the broader field of advanced materials for many application sectors (not just electronics). At the same time, ALD depends on advances in fields like metrology, modelling, surface science and plasma physics. This will also be true of the emerging new fields of ALEt and selective-area processing presented here. We therefore mention three associated areas that should be developed in tandem:

- Atomic-level metrology such as mass spectrometry, mass sensing and optical methods with enhanced sensitivity;
- Atomic Layer Cleaning – wet chemical processing with atomic level control and enhanced material selectivity;
- Atomic-level control in the processing of 2D materials;
- III-V semiconductor nanowire-based quantum computing.

6 Wider context

6.1 Supply chain for materials processing

Atomic-level processing will be a multi-disciplinary effort encompassing chemical synthesis, surface and vacuum science, materials characterization, process engineering and application fields such as electronic engineering or renewable energy. Progress will therefore only be possible through a properly integrated R&D effort across the full supply chain. This will be true both in laboratory research (low technology readiness level, TRL) and when moving to commercialization (high TRL), as illustrated in Figure 3 below.

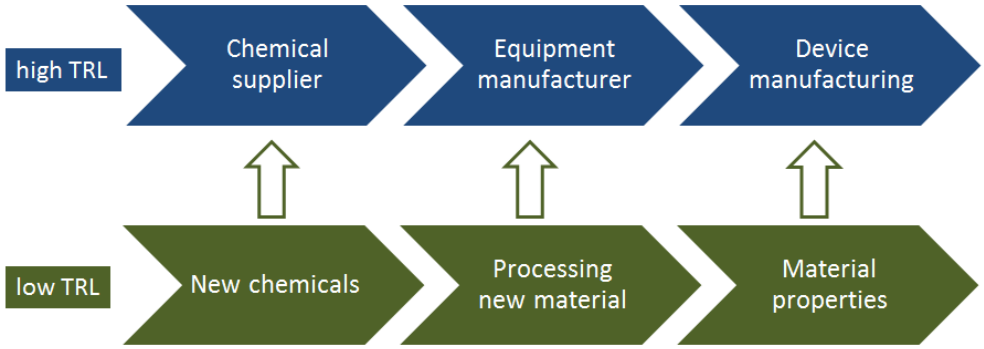

Figure 3: Simplified supply chain for materials processing at both lab scale (green) and industrial scale (blue). Not shown are the many other supply chains that feed into each segment: for example, vacuum components are supplied to equipment manufacturers.

Many breakthroughs in ALD processing have been successfully transferred from academic labs to high-volume manufacturing, often because of the strong commitment of companies in this field to collaborative R&D.

6.2 Relation to other European initiatives

The European Technology Platform for Advanced Engineering Materials and Technologies recognizes[7] that processing and production technologies are the main obstacle to be overcome in realizing the commercial potential of nanotechnology in Europe:

> "Today the main general challenge is to concentrate the resources to create novel production processes as a part of a complete value chain of product."

The atomic-level processing R&D goals proposed here are concrete examples of the 3-5 year and 5-10 year objectives outlined by EuMaT relating to nanomaterials.

7 Acknowledgements

COST Action MP1402 '*Hooking together European research in atomic layer deposition*' (HERALD) is a network of 160 researchers from 29 European countries and 6 partner countries worldwide, including universities, research institutes, multi-national companies and SMEs; http://www.european-ald.net/

HERALD is open to all ALD researchers from the member countries and aims to provide an open and neutral forum for collaboration and the exchange of latest research findings. Members include universities, research institutes and companies representing the complete supply chain for materials processing – precursor suppliers, equipment manufacturers (three out of the four leading companies worldwide) and high-tech manufacturing (especially in the semiconductor and renewable energy sectors). The contributions to this white paper from HERALD's academic and industrial members are gratefully acknowledged.

COST (European Cooperation in Science and Technology) is a pan-European intergovernmental framework. Its mission is to enable break-through scientific and technological developments leading to new concepts and products and thereby contribute to strengthening Europe's research and innovation capacities. It allows researchers, engineers and scholars to jointly develop their own ideas and take new initiatives across all fields of science and technology, while promoting multi- and interdisciplinary approaches. COST aims at fostering a better integration of less research intensive countries to the knowledge hubs of the European Research Area. The COST Association, an international not-for-profit association under Belgian law, integrates all management, governing and administrative functions necessary for the operation of the framework. The COST Association has currently 36 member countries. www.cost.eu

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